AMENDMENTS TO THE CLAIMS

Please amend Claims 1, 2, 4, 5, and 7, and add new Claims 30-40. Claims 3, 6, 8, and 9 remain as previously pending.

1. (Currently Amended) An electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; ~~and~~

a switch configured to decouple said data bus from said memory circuit; when no memory access is being requested by said memory controller ~~so as~~ to reduce the parasitic capacitance of said data bus, wherein the switch is an integrated part of the memory circuit; and

a state decoder interfaced with the memory controller, wherein the state decoder selectively controls the switch.

2. (Currently Amended) The electronic device of Claim 1 further comprising a plurality of memory circuits and a corresponding plurality of ~~decoupling means~~switches.

3. (Original) The electronic device of Claim 1, wherein the memory circuit comprises a synchronous DRAM memory.

4. (Currently Amended) An electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; ~~and~~

a switch configured to decouple said data bus from said memory circuit when no memory access is being requested by said memory controller ~~so as~~ to reduce the parasitic capacitance of said data bus~~,~~; and

a state decoder interfaced with the memory controller, wherein the state decoder selectively controls the switch;

wherein the switch, the memory circuit, and the ~~memory controller~~state decoder are integrated into a single circuit.

5. (Currently Amended) The electronic device of Claim 4, additionally comprising a plurality of memory circuits and a corresponding plurality of ~~decoupling means~~switches.

6. (Original) The electronic device of Claim 4, wherein the memory circuit comprises a synchronous DRAM memory.

7. (Currently Amended) An electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a decoupling means ~~switch~~ configured to decouple said data bus from said memory circuit when no memory access is being requested by said memory controller ~~so as~~ to reduce the parasitic capacitance of said data bus,

a state decoder interfaced with the memory controller, wherein the state decoder selectively controls the decoupling means;

wherein the ~~switch~~decoupling means, the memory circuit and the ~~memory controller~~ state decoder are integrated into a single circuit.

8. (Original) The electronic device of Claim 7, comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

9. (Original) The electronic device of Claim 7, wherein the memory circuit comprises a synchronous DRAM memory.

10. -29. (Canceled)

30. (New) The electronic device of Claim 1 wherein the switch is a transfer gate.

31. (New) The electronic device of Claim 1 further comprising interfacing the state decoder with the switch.

32. (New) The electronic device of Claim 1 further comprising an address signal wherein the state decoder decodes the address signal to determine whether the memory access is occurring.

33. (New) The electronic device of Claim 32 wherein the address signal is a column address.

34. (New) The electronic device of Claim 4 wherein the switch is a transfer gate.

35. (New) The electronic device of Claim 4 further comprising interfacing the state decoder with the switch.

36. (New) The electronic device of Claim 4 further comprising an address signal wherein the state decoder decodes the address signal to determine whether the memory access is occurring.

37. (New) The electronic device of Claim 36 wherein the address signal is a row address.

38. (New) The electronic device of Claim 7 further comprising interfacing the state decoder with the decoupling means.

39. (New) The electronic device of Claim 7 further comprising an address signal wherein the state decoder decodes the address signal to determine whether the memory access is occurring.

40. (New) The electronic device of Claim 39 wherein the address signal is a row address.